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EXAMINER

VU, TRISHA U

ART UNIT

PAPER NUMBER

2112

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/736,582

Applicant(s)

HOFSTEE ET AL.

Examiner

Trisha U. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 11, 13-19, 24-26, 28, 29 and 31 is/are rejected.
- 7) ☒ Claim(s) 8-10, 12, 20-23, 27, 30 and 32-36 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-36 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 4-7, 11, 13, 16-19, 24-25, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein after AAPA) in view of Gentry, Jr. et al. (6,467,008) (herein after Gentry).

As to claim 1, AAPA teaches a system comprising a shared memory (shared memory); and a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit (CPU), a direct memory access controller (DMA controller) and a plurality of attached processing units (APUs), wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein each of said plurality of attached processing units interrupts said corresponding processing unit upon completion of each of said one or more remote procedure calls (pages 2-3). AAPA does not explicitly disclose each of said

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plurality of attached processing units does not interrupt said corresponding processing unit upon completion of each of said one or more remote procedure calls. Gentry teaches using polling technique to eliminate interrupts in a system (col. 6, lines 10-18 and col. 14, lines 9-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling in place of interrupts as taught by Gentry in the system of AAPA to improve the system performance since in heavy traffic the amount of time a host processor may spend processing interrupts may degrade a host computer's responsiveness to other tasks (col. 14, lines 9-11).

As to claim 13, AAPA teaches a system comprising a shared memory (shared memory); and a plurality of processing elements coupled to said shared memory, wherein each of said plurality of processing elements comprises a processing unit (CPU), a direct memory access controller (DMA controller) and a plurality of attached processing units (APUs), wherein said direct memory access controller is configured to receive a plurality of commands from a corresponding processing unit to be executed during one or more remote procedure calls, wherein said plurality of APUs interrupts said corresponding processing unit upon completion of each of said one or more remote procedure calls (pages 2-3). AAPA does not explicitly disclose the direct memory access controller is configured to poll a status line of each of said plurality of APUs to determine if any of said plurality of APUs completed its operation during said one or more remote procedure calls. Gentry teaches using polling technique to eliminate interrupts in a system (col. 6, lines 10-18 and col. 14, lines 9-23). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement polling in place of interrupts

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as taught by Gentry in the system of AAPA to improve the system performance since in heavy traffic the amount of time a host processor may spend processing interrupts may degrade a host computer's responsiveness to other tasks (col. 14, lines 9-11).

As to claim 24, AAPA teaches a method for executing one or more remote procedure calls comprising the steps of: issuing a plurality of commands by a processing unit (CPU) to a direct memory access controller (DMA controller) to be executed during one or more remote procedure calls, wherein said plurality of commands comprise a first instruction to copy attached processing unit instructions (issuing a command to the DMA controller to copy a certain code) associated with a particular attached processing unit (APU) from a memory (shared memory) to said particular attached processing unit, wherein said plurality of commands comprise a second instruction to copy data (issuing a command to the DMA controller to copy data) associated with said APU instructions from said memory to said particular APU; issuing to said particular APU an indication to start a particular operation on said data (start the operation on the particular data) associated with said particular APU instructions, wherein said plurality of APUs interrupts said corresponding processing unit upon completion of each of said one or more remote procedure calls (pages 2-3). AAPA does not explicitly disclose the plurality of APUs do not interrupt said processing unit upon completion of each of said one or more remote procedure calls and polling a status line of each of a plurality of APUs to determine if any of said plurality of attached processing units completed its particular operation. Gentry teaches using polling technique to eliminate interrupts in a system (col. 6, lines 10-18 and col. 14, lines 9-23). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to implement polling in place of interrupts as taught by Gentry in the system of AAPA to improve the system performance since in heavy traffic the amount of time a host processor may spend processing interrupts may degrade a host computer's responsiveness to other tasks (col. 14, lines 9-11).

As to claims 4, 16, AAPA further teaches the plurality of commands comprise a first instruction to copy APU instructions (issuing a command to the DMA controller to copy a certain code) associated with a particular APU from said shared memory to said particular APU, wherein said plurality of commands comprise a second instruction to copy data (issuing a command to the DMA controller to copy data) associated with said APU instructions from said shared memory to said particular APU (pages 2-3).

As to claims 5, 17, AAPA further teaches the APU instructions associated with said particular APU comprise instructions that enable said particular APU to perform a particular operation on said data (start the operation on the particular data) associated with said APU instructions associated with said particular APU (page 3).

As to claims 6, 18, AAPA further teaches the plurality of commands comprise a third instruction to copy the results of said particular operation (resulting data) to said shared memory (page 3).

As to claims 7, 19, 31, AAPA further teaches the first and second instructions are requests to copy one or more lines of memory in said shared memory to said particular attached processing unit (pages 2-3).

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As to claim 11, AAPA as modified by Gentry above further teaches polling instead of using interrupts to determine if any of said plurality of APUs completed its operation during said on or more remote procedure calls (col. 6, lines 10-18 and col. 14, lines 9-23).

As to claims 12, 23, and 27, AAPA does not explicitly disclose interrupting the processing unit at a synchronization point, wherein said synchronization point after said one or more remote procedure calls are performed. Gentry teaches providing interrupt at a synchronization point (at least a period of time) after polling for a number of packets (abstract and col. 3, lines 26-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include providing interrupt at a synchronization point as taught by Gentry in the system of AAPA so that the overhead of processing a separate polling operation or interrupt for each event is avoided.

As to claim 25, AAPA further teaches the APU instructions enable said particular APU to perform said particular operation (start the operation on the particular data) (page 3).

3. Claims 2-3, 14-15, 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein after AAPA) in view of Gentry, Jr. (6,434,651) (herein after Gentry) as applied to claims 1, 13 and 24 above, and further in view of Goyal et al. (6,055,579) (herein after Goyal).

As to claims 2-3, 14-15, 28-29, AAPA and Gentry do not explicitly disclose a plurality of first level queues for storing said plurality of commands issued by said

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corresponding processing unit, wherein each of said plurality of first level queues are configured to store one or more commands of said plurality of commands associated with a different attached processing unit. Goyal teaches a plurality of command queues for storing the commands associated with different attached processing units (processing engines) (at least col. 10, lines 55-62, col. 3, lines 1-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement command queues for storing the commands associated with different attached processing units as taught by Goyal in the system of AAPA and Gentry to at least resolve data dependencies between the processing units (by conditionally queue technique) (at least col. 3, lines 1-6).

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein after AAPA) in view of Gentry, Jr. (6,434,651) (herein after Gentry) as applied to claim 24 above, and further in view of Orr et al. (4,862,350) (herein after Orr).

As to claim 26, AAPA and Gentry do not explicitly disclose the indication to start said particular operation on said data is issued from said direct memory access controller to said particular APU. Orr teaches issuing commands/messages from a direct memory access controller (Units 32 and 20) instead of directly from the primary processor (col. 5, lines 49-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include issuing commands/messages from a direct memory access controller as taught by Orr in the system of AAPA and Gentry to free the primary processor for other operations.

Allowable Subject Matter

5. Claims 8-10, 20-22, 30, 32-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 8, 20, and 30 include the limitation of the direct memory access controller comprises a second queue, wherein the plurality of commands in the plurality of first queues are merged in said second queue, which is not shown by the prior art of record, in the combination as disclosed and claimed.

Claim 34 includes the limitation of the memory access controller comprises a second queue, wherein the plurality of commands in the plurality of first queues are expanded in said second queue, which is not shown by the prior art of record, in the combination as disclosed and claimed.

Response to Arguments

Applicant's arguments filed 03-22-04 have been fully considered but they are not persuasive:

With respect to Applicants' arguments on pages 3-5 of the Remarks that "*The examiner must provide evidence as to why one of ordinary skill in the art with a primary reference (Applicants' Background) in front of him, which teaches a symmetric multi-processing computer architecture, would be modified with a secondary reference (Gentry) which teaches a network*

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interface polled by a process operating on a host computer system.”: it is noted that Applicants’ Background teaches all the limitations in the claim except polling for completion of the remote procedure calls. Therefore, only the polling method in Gentry is used in the system of Applicants’ Background, not the network environment as argued by Applicant. Note in here that only the teaching of what is missing in Applicants’ Background system is brought into the system, not the whole secondary reference. And also, since this is a polling method, the examiner believes that it is usable in any computer environment. Also, note that the motivation is found in Gentry reference itself as addressed in the rejection above so as to improve the system performance in large amount of traffic by using polling in place of interrupts.

With respect to Applicants’ arguments of claims 12, 23, and 27 on pages 5-6 of the Remarks that “*Gentry does not teach that this interrupt is generated after one or more remote procedure calls are performed*”, note that “the one or more remote procedure calls are performed” is already taught in Application’s Background, and Gentry further teaches generating interrupt to the host processor at a synchronization point (after a maximum number of packets be received). Thus, it would have been obvious to implement generating interrupt to the host processor at a synchronization point as taught by Gentry in the system of Applicant’s Background so that the overhead of processing a separate polling operation or interrupt for each event is avoided. Applicant further stated that “This motivation is insufficient for a prima facie case of obviousness since it is merely the Examiner’s subjective opinion without any support from objective evidence”. It is noted that Gentry had mentioned the problem in the prior art that an interrupt is issued to the processor for each packet transferred, and when numerous interrupts are issued, the processor must spend more time on context switches and processing the interrupt

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(col. 2, lines 5-17). Therefore, generating an interrupt after a number of events is to avoid the overhead of processing interrupt for each individual event.

With respect to Applicants' arguments on pages 7-8 of the Remarks that "*Applicants' Background teaches a symmetric multiprocessing computer system... Goyal, on the other hand, teaches a system for synchronization of data processing in a data processing system including multiple command queues*", it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). Note that Goyal teaches "The invention can be readily implemented in any data processing system or subsystem with one or more processing engines" (col. 3, lines 7-14). Therefore, the command queues associated with the processing units (processing engines) as taught by Goyal are applicable in the plurality of processing units of Applicants' Background to resolve data dependencies between the processing units. In response to applicant's argument that the motivation is insufficient to support a *prima facie* case of obviousness since its is merely the Examiner's subjective opinion, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation is found in Goyal reference itself as addressed in the rejection above.

With respect to Applicants' arguments of claim 26 on page 9 of the Remarks that the motivation "to free the primary processor for other operations" is merely the Examiner's subjective opinion, again the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it is well known in the art to provide a DMA controller is to free the processor for other operations.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Trisha U. Vu
Examiner
Art Unit 2112

uv


SUMATI LEFKOWITZ
PRIMARY EXAMINER